Toward Low-Power Electronics: Tunneling Phenomena in Transition Metal Dichalcogenides

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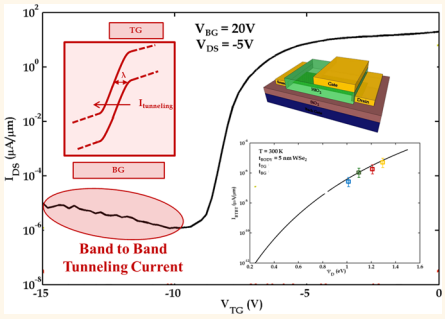
ABSTRACT In this article, we explore, experimentally, the impact of band-to-band tunneling on the electronic transport of double-gated WSe_2 field-effect transistors (FETs) and Schottky barrier tunneling of holes in back-gated MoS_2 FETs. We show that by scaling the flake thickness and the thickness of the gate oxide, the tunneling current can be increased by several orders of magnitude. We also perform numerical calculations based on Landauer formalism and WKB approximation to explain our experimental findings. Based on our simple model, we discuss the impact of band gap and effective mass on the band-to-band tunneling current and evaluate the performance limits for a set of dichalcogenides in the context of tunneling transistors for low-power applications. Our findings suggest that WTe_2 is an excellent choice for tunneling field-effect transistors.



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For decades, the semiconductor industry has been driven by the central objective of scaling down the channel dimensions of transistors in order to enhance their speed and packing densities while preserving an inverse subthreshold swing (defined as the gate voltage required to change the drain current by an order of magnitude) close to 60 mV/decade to minimize the power dissipation.[1−3] While silicon has successfully been used in this context in the past, novel low-dimensional materials that encompass semiconducting nanowires,[4,5] nanotubes,[6,7] III−V compound semiconductors,[8] graphene,[9,10] and more recently the large family of transition metal dichalcogenides such as MoS_2, WSe_2, and others[11−14] are now frequently discussed as options for continued scaling beyond the 10 nm technology node. Moreover, recent developments indicate that innovative device ideas that include tunneling field-effect transistors (TFETs),[15−18] impact ionization MOS devices,[19,20] suspended gate FETs,[21] and ferroelectric FETs[22] offer an opportunity to operate below the 60 mV/decade limit. Combining low-dimensional materials with these new concepts is thus a promising route toward new generations of electronic devices.

In this article, we evaluate the potential of transition metal dichalcogenides in the context of TFETs. In particular, first, we demonstrate Schottky barrier tunneling of holes in MoS_2 and band-to-band tunneling in WSe_2 and then use these experimental findings along with analytical calculations to make projections for TFETs based on various dichalcogenides.

RESULTS AND DISCUSSION

Schottky Barrier Tunneling of Holes in MoS_2. MoS_2 along with other transition metal dichalcogenides has generated a lot of interest in the device community due to their excellent electrostatic integrity that allows for aggressive channel length scaling. These novel two-dimensional layered semiconductors are naturally occurring ultrathin body materials similar to graphene, but with the added advantage of having a significant band gap which is essential for logic applications.[23−26] Numerous articles have been published arguing about the potential of MoS_2 for future nanoelectronics applications.[27−31] In our earlier reports, we have

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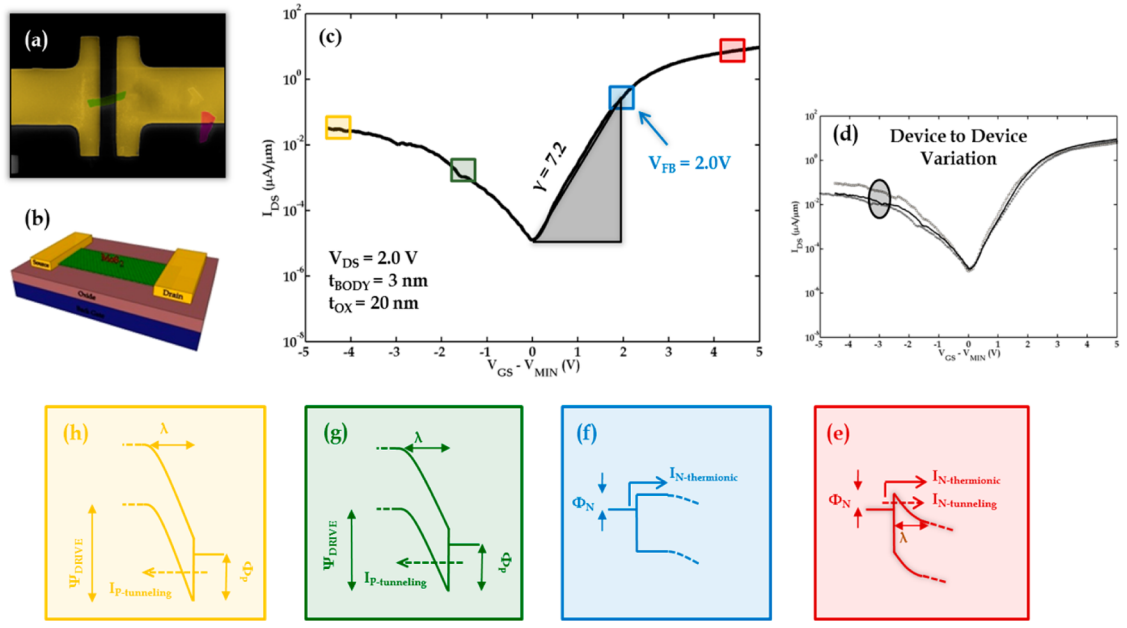


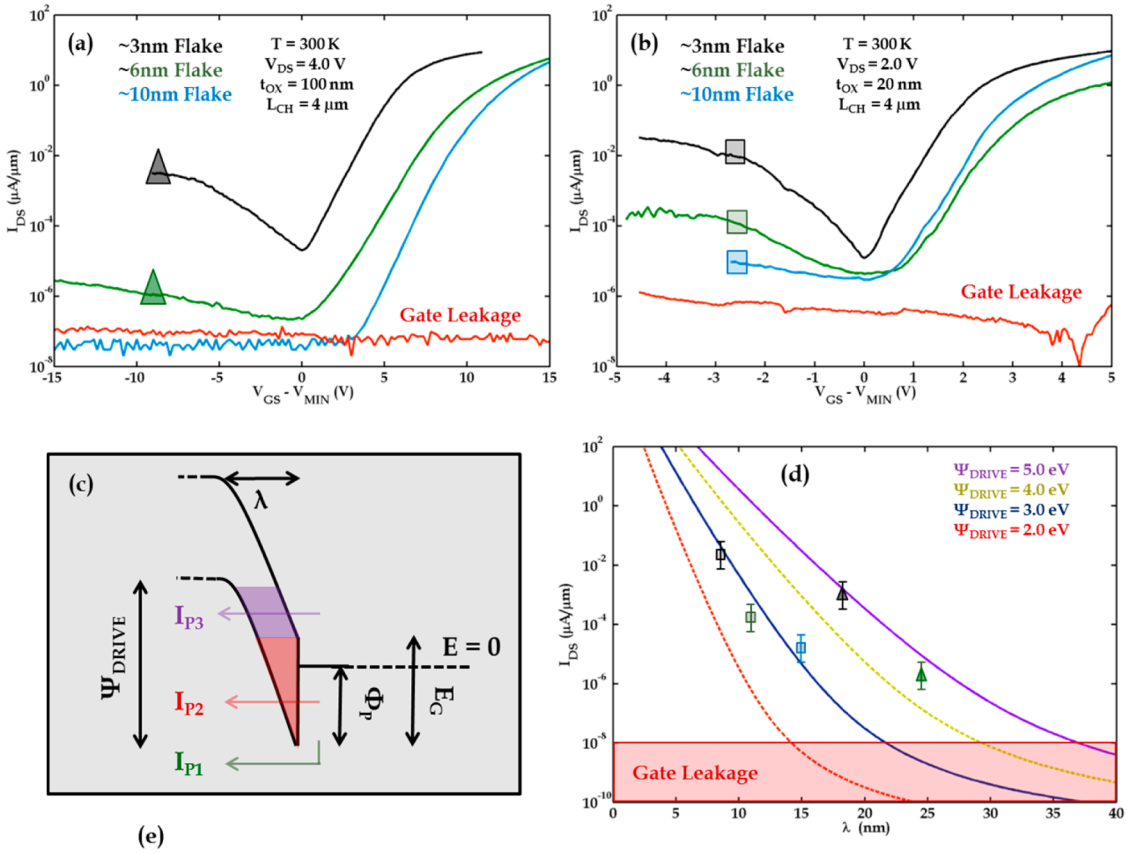
Figure 1. (a) False color optical image and (b) 3-D cartoon of a prototype back-gated MoS_2 FET. (c) Transfer characteristics of representative ~3 nm thick MoS_2 FET with Pd as source/drain contact electrodes and 20 nm SiO_2 as back gate. (d) Transfer characteristics of several ~3 nm thick MoS_2 FETs illustrating device-to-device variations. (e−h) Energy band diagrams corresponding to different gate bias conditions marked in different color boxes in panel c.

evaluated several key aspects related to transistor design and carrier transport through MoS_2-based FETs such as contact formation,[31] optimum layer thickness evaluation,[32] channel length scaling, and current distribution among the individual layers of multilayer MoS_2.[33,34] However, in all these articles, we have focused on the electron transport through the MoS_2 FETs due to the absence of an appreciable hole branch in the device characteristics at negative gate voltages. Strong Fermi level pinning close to the conduction band of MoS_2 had been responsible for this experimental finding as it results in a large Schottky barrier height for hole injection into the valence band of MoS_2. In this article, we show that by proper choice of flake thickness, oxide thickness, and biasing conditions, hole currents can be injected into the valence band of MoS_2 through tunneling. This tunneling, as mentioned before, occurs through a large Schottky barrier height which is similar to the band gap of this material and hence allows us to evaluate the potential of MoS_2 in the context of TFETs.

Figure 1a shows a false color optical image, and Figure 1b shows the 3-D device structure schematically of a prototype back-gated MoS_2 FET used for our tunneling study. The 20 and 100 nm silicon dioxide (SiO_2) substrates with underlying highly doped silicon were used as the back gate and palladium (Pd) with a subnanometer adhesive layer of titanium (Ti) was used as the source/drain metal contact. The channel length for all the devices was designed to be 4 μm.

Figure 1c shows room temperature transfer characteristics of a representative device, and Figure 1d indicates how much device-to-device variations impact the current of ~3 nm thick MoS_2 FETs with 20 nm thick SiO_2 as the back gate oxide. Figure 1e−h illustrates the energy band diagrams corresponding to different gate biases (shown in semitransparent square boxes in Figure 1c) qualitatively. A large positive voltage was applied to the drain terminal (V_{DS} = 2.0 V) to facilitate hole injection from the drain terminal (Figure 1g,h). For large positive gate biases ($V_{GS} > V_{FB}$, where V_{FB} is the flat band voltage), electrons are injected into the channel from the source terminal (Figure 1e). This electron current has two components—thermionic emission current over the top of the Schottky barrier ($I_{N\text{-thermionic}}$) and the tunneling current through the Schottky barrier ($I_{N\text{-tunneling}}$). As V_{GS} is reduced to V_{FB}, the electron tunneling current vanishes, as shown in Figure 1f. For $V_{GS} < V_{FB}$, the thermionic emission current starts to drop exponentially and the device enters into its OFF state. As V_{GS} is further reduced, holes can tunnel into the channel through the Schottky barrier at the drain terminal (Figure 1g). Note that the height of the Schottky barrier for hole injection into the valence band is $\Phi_P = E_G - \Phi_N$, where E_G is the band gap of MoS_2 and Φ_N is the Schottky barrier height for electron injection into the conduction band which had been determined previously by us as ~250 meV for Pd on MoS_2.[31]

Figure 2a shows the room temperature transfer characteristics of 3, 6, and 10 nm thick MoS_2 FETs back-gated through a 100 nm SiO_2 film. For the 10 nm thick MoS_2 flake, the hole tunneling current is below the noise floor for the entire range of V_{GS} and



t_{OX} (nm)	t_{BODY} (nm)	V_{FB} (V)	V_{GS} - V_{MIN} (V)	γ	V_{DS} (V)	$\Psi_{DRIVE} = qV_{DS} + q\lvert(V_{GS} - V_{MIN} - V_{FB})/\gamma\rvert$ (eV)	λ(nm)
100	6	5.0	-9.0	21.0	4.0	**4.7** (~ 5.0)	24.5
	3	8.0	-9.0	18.5	4.0	**4.9** (~ 5.0)	17.3
20	10	2.8	-2.7	7.6	2.0	**2.7** (~ 3.0)	14.1
	6	2.6	-2.7	7.5	2.0	**2.7** (~ 3.0)	10.9
	3	1.8	-2.7	7.2	2.0	**2.6** (~ 3.0)	7.7

Figure 2. Room temperature transfer characteristics of a 3, 6, and 10 nm thick MoS_2 FET with Pd as source/drain contact electrodes on (a) 100 nm and (b) 20 nm SiO_2 as the back gate dielectric. (c) Simplified energy band diagram used to calculate the tunneling current within WKB approximation. (d) Experimental (squares and triangles) and simulated (solid lines) tunneling currents as a function of the screening length (λ) for different drive voltages (Ψ_{DRIVE}). (e) Table showing the extracted Ψ_{DRIVE} values from panels a and b.

was not used in our quantitative analysis. For the 6 and 3 nm thick MoS_2 flakes, the hole tunneling current, as expected, increased monotonically with the applied V_{GS}. The hole tunneling current was found to be ~1 × 10^{-6} and ~3 × 10^{-3} μA/μm for the 6 and 3 nm flakes, respectively, for $V_{GS} - V_{MIN} = -9.0$ V. Figure 2b shows room temperature transfer characteristics of MoS_2 FETs for similar flake thicknesses but back-gated through a 20 nm SiO_2 layer. The hole tunneling currents in this case were found to be ~9 × 10^{-6}, ~1 × 10^{-4}, and ~1 × 10^{-2} μA/μm for 10, 6, and 3 nm flakes, respectively, for $V_{GS} - V_{MIN} = -2.7$ V. Our experimental data suggest that the tunneling current can be enhanced by scaling the oxide thickness and the flake thickness. In order to understand the magnitude of the hole tunneling currents, we have performed numerical calculations based on a simple analytical model described in the following equations.[16,35,36]

$$I_{P1} = q\int_{\Phi_p}^{\infty} M(E + \Psi_{DRIVE} - \Phi_p)f(E)dE \quad (1a)$$

$$I_{P2} = q\int_{\Phi_p - E_G}^{\Phi_p} M(E + \Psi_{DRIVE} - \Phi_p)T_{WKB-2}(E)f(E)dE \quad (1b)$$

$$I_{P3} = q\int_{\Phi_p - \Psi_{DRIVE}}^{\Phi_p - E_G} M(E + \Psi_{DRIVE} - \Phi_p)T_{WKB-3}(E)f(E)dE \quad (1c)$$

$$M(E) = \frac{2}{h^2}\sqrt{2m_pE},\ f(E) = \frac{1}{1 + \exp\left(\frac{E}{k_BT}\right)} \quad (1d)$$

$$T_{WKB-2}(E) = \exp\left(-\frac{8\pi}{3h}\sqrt{2m_p(\Phi_p - E)^3}\,\frac{\lambda}{\Psi_{DRIVE}}\right) \quad (1e)$$

$$T_{WKB-3}(E) = \exp\left(-\frac{8\pi}{3h}\sqrt{2m_p E_G^3}\,\frac{\lambda}{\Psi_{DRIVE}}\right) \quad (1f)$$

$$\lambda = \sqrt{t_{ox}t_{body}\,\frac{\varepsilon_{body}}{\varepsilon_{ox}}} = \sqrt{t_{ox}t_{body}\,\frac{\varepsilon_{environment}}{\varepsilon_{ox}}}$$
$$\approx \sqrt{t_{ox}t_{body}} \quad (1g)$$

We have used Landauer formalism in order to calculate both the thermionic (I_{P1}) and the tunneling (I_{P2} and I_{P3}) components of the source to drain current in units of A/m. In the above equations, q is the electronic charge, h is the Plank constant, k_B is Boltzmann constant, and T is the temperature. $M(E)$ (in units of $(eV\cdot m\cdot s)^{-1}$) is the number of conducting modes (product of the density of states $D(E)$ and the average velocity $v(E)$) in the channel of the transistor corresponding to a 2-D parabolic band structure; $f(E)$ is the Fermi distribution, and $T_{WKB-2}(E)$ and $T_{WKB-3}(E)$ are the tunneling probabilities corresponding to the two different regimes shown in Figure 2c. WKB approximation for a triangular potential barrier has been used to calculate the tunneling probabilities. Ψ_{DRIVE} is defined as the potential in the channel of the transistor corresponding to the applied gate and drain biases (see also definition in the table of Figure 2e and discussion below); λ is the geometric screening length; m_p, ε_{body}, and t_{body} are the effective mass, in-plane (in the direction of transport) dielectric constant, and thickness of the channel material, respectively, and ε_{ox} and t_{ox} are the dielectric constant and the thickness of the gate oxide. For an ultrathin body channel material, the field lines between the source and the drain contacts lie more in the environment rather than inside of the channel, and therefore, ε_{body} should be replaced by $\varepsilon_{environment}$, which in back-gated transistor geometry can be assumed to be the average of the dielectric constant of air, ε_{body} and ε_{ox}. For our calculations, we have used $m_p = 0.57m_0$, $\varepsilon_{body} = 7.0$, $\varepsilon_{ox} = 3.9$, $E_G = 1.2$ eV, and $\Phi_p = 0.95$ eV.[25,31]

Figure 2d shows the Schottky barrier tunneling current (solid curves) as a function of the geometric screening length (λ) for different Ψ_{DRIVE} values. Figure 2d also shows the experimental data (semitransparent squares and triangles) corresponding to the different oxide thicknesses and flake thicknesses extracted from Figure 2a,b. Error bars capture device-to-device variations as shown in Figure 1d. It is interesting to note that the experimental data corresponding to 100 nm back gate oxide for different flake thicknesses lie close to the contour Ψ_{DRIVE} = 5.0 V, and the experimental data corresponding to 20 nm back gate oxide for different flake thicknesses lie close to the contour Ψ_{DRIVE} =3.0 V in Figure 2d. In order to understand this finding, we calculated the magnitudes of Ψ_{DRIVE} from our experimental data using the following procedure.

1. Determination of V_{FB}: The flat band voltage is defined as the gate bias at which the electron tunneling current from the source terminal is completely blocked and the device current is determined only by the thermionic emission over the top of the Schottky barrier (Figure 1f). For $V_{GS} < V_{FB}$, the slope of the log I_{DS} *versus* V_{GS} curve is a constant and is equal to 60γ mV/decade (where γ is the band movement factor defined next). V_{FB}, therefore, can be approximately determined by finding the point on the subthreshold regime of the device characteristics where the slope changes from being constant (blue semitransparent dot in Figure 1c).

2. Determination of γ: In a field-effect transistor, the band movement in the channel is determined by factor $\gamma = [1 + (C_{it} + C_{ch})/C_{ox}]$, where C_{it}, C_{ch}, and C_{ox} are the interface trap capacitance, channel capacitance, and oxide capacitance, respectively. In the subthreshold regime of the device operation, C_{ch} is negligible and, therefore, the band movement factor remains constant and gets reflected in the subthreshold slope as 60γ mV/decade. Therefore, from the constant slope of the log I_{DS} *versus* V_{GS} curve, the magnitude of γ can be extracted (see the semitransparent black right angled triangle in Figure 1c).

3. Determination of Ψ_{DRIVE}: Once V_{FB} and γ are extracted, the band position in the channel can be determined from the relation $\Psi_{DRIVE} = qV_{DS} + q|(V_{GS} - V_{min} - V_{FB})/\gamma|$. The reader should note that the band movement factor has been assumed to be the same for both the electron branch and the hole tunneling regime in the device characteristics. This assumption occurs justified because the amount of tunneling charges in the channel of the transistor remains small enough to ignore the contribution of the quantum capacitance (C_{ch}) even for large negative V_{GS}. Moreover, since the Schottky barrier for hole injection is significantly larger than for electron injection, most of the drain voltage drop will occur close to the drain where the larger Schottky barrier results in a smaller transmission probability.

Table in Figure 2e shows the Ψ_{DRIVE} values obtained for the different MoS_2 transistors after extracting the flat band voltage V_{FB} and the band movement factor γ from the experimental transfer characteristics shown in Figure 2a,b. Clearly, our first-order analysis agrees well with the numerical calculations. Note that large V_{DS} values were used to enhance the channel potential Ψ_{DRIVE}, which is not desirable for conventional transistor operation since the channel potential should be under gate control. However, this approach allows us here to demonstrate in a simple way tunneling through a large Schottky barrier as well as to study the impact of scaling on the tunneling current density.

Band-to-Band Tunneling in WSe_2. WSe_2 is another member of the transition metal dichalcogenides family which also is promising for certain next generation electronic applications.[13,37] Previously, we had demonstrated that, unlike MoS_2, the Fermi level pinning at the

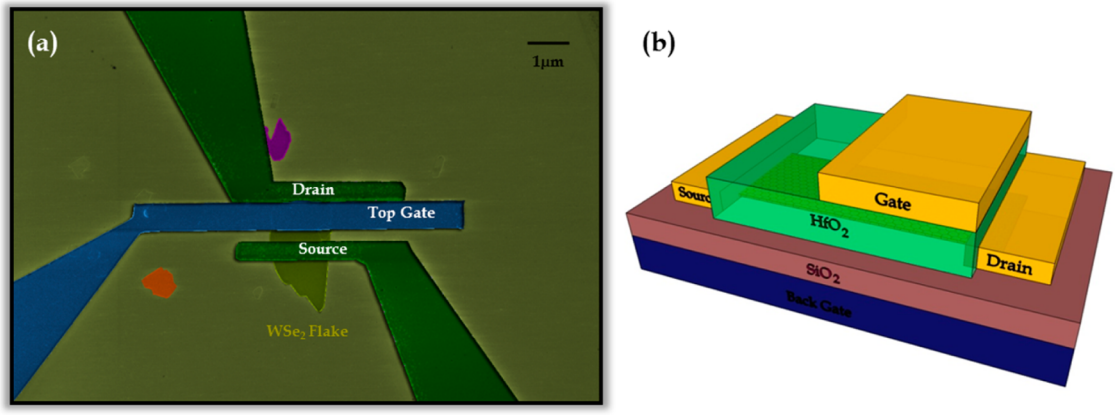


Figure 3. (a) SEM image and (b) 3-D cartoon of a 5 nm thick WSe_2 FET with partial top gate and full bottom gate.

metal to WSe_2 interface is close to the middle of the band gap of WSe_2,[38] which allows for both electron and hole injection into the respective energy bands.[38] If a p-n junction is created along a WSe_2 channel through electrostatic doping, the above implies that source and drain can populate the channel with both electrons and holes. Moreover, the electron and hole effective masses for the tungsten dichalcogenides are smaller compared to most of the other group VI metal chalcogenides, which is expected to result in an enhanced tunneling probability. For our first band-to-band tunneling demonstration, we thus chose WSe_2 and adjusted the threshold voltages of the two halves of the same channel to make one region n-type and the other p-type using a partial top gate and full bottom gate geometry as shown in the SEM image and the 3D cartoon in Figure 3.

90 nm silicon dioxide (SiO_2) substrate with underlying highly doped silicon was used as the back gate, and a stack of Ti/Pd was used as the source/drain metal contact. Flake of thicknesses ~5 nm were selected for the fabrication of the band-to-band tunneling devices. The 30 nm HfO_2 was deposited as the top gate dielectric using atomic layer deposition technique. The p and n regions of the device were created through electrostatic doping and could be independently controlled through the use of a partial top gate in conjunction with a full back gate as shown in Figure 3. This design allows one portion of the channel to be controlled only by the back gate, while the rest of the channel is jointly controlled by the back gate and the top gate. The entire channel of the device was 1 μm long, while the top-gated portion was 500 nm long.

Figure 4a shows room temperature back-gated transfer characteristics of a WSe_2 transistor. For positive back gate voltage ($V_{BG} > 0$), electrons are injected into the channel through the triangular Schottky barrier at the drain terminal (note that negative V_{DS} is applied), and for negative back gate voltage ($V_{BG} < 0$), holes are injected into the channel through the triangular Schottky barrier at the source terminal. The corresponding energy band diagrams for the electron and the hole injections are shown in Figure 4b,c. The Schottky barrier heights for the electron and the hole injection at the Ti/Pd to WSe_2 contacts were found to be $\Phi_N = 0.52$ eV and $\Phi_p = 0.68$ eV, respectively, using a similar technique as described in our earlier article.[38] Since the Schottky barrier height for the hole injection is higher than that for the electron injection, the hole current (at negative gate voltages) is smaller than the electron current for similar gate over drive voltages. Note that the thermionic component of the current for both the electrons and the holes are expected to be negligible compared to the corresponding thermally assisted tunneling component due to significant Schottky barriers at the source- and drain-to-channel interface.

Figure 4e shows room temperature transfer characteristics of a partially top-gated WSe_2 FET corresponding to two different back gate biases. Figure 4f,g shows the energy band diagrams associated with different regions of the device operation. Positive back gate biases were used to facilitate the injection of electrons into the channel. The role of the partial top gate is to control the bands in the top-gated region and thereby modulate the channel current. For positive or small negative top gate voltages, V_{TG}, the top-gated region remains n-doped (since the back gate bias is still in effect) and the device exhibits electron conduction. This is also clear from the fact that at a more positive back gate voltage (V_{BG1}) the whole $I_{DS}-V_{TG}$ curve (black) shifts up compared to one at lower back gate voltage (V_{BG2}) (green curve) as well as the shift of threshold voltage. As V_{TG} is made more negative, the bands in the top-gated region move up and block the electron current injected from the drain terminal. This turns the device off. As V_{TG} becomes more negative, electrons occupying the valence band in the top-gated region start to tunnel through the band gap into the conduction band region that is controlled by the back gate. This results in an increase in the device current, as shown in Figure 3e. The reader might argue that this

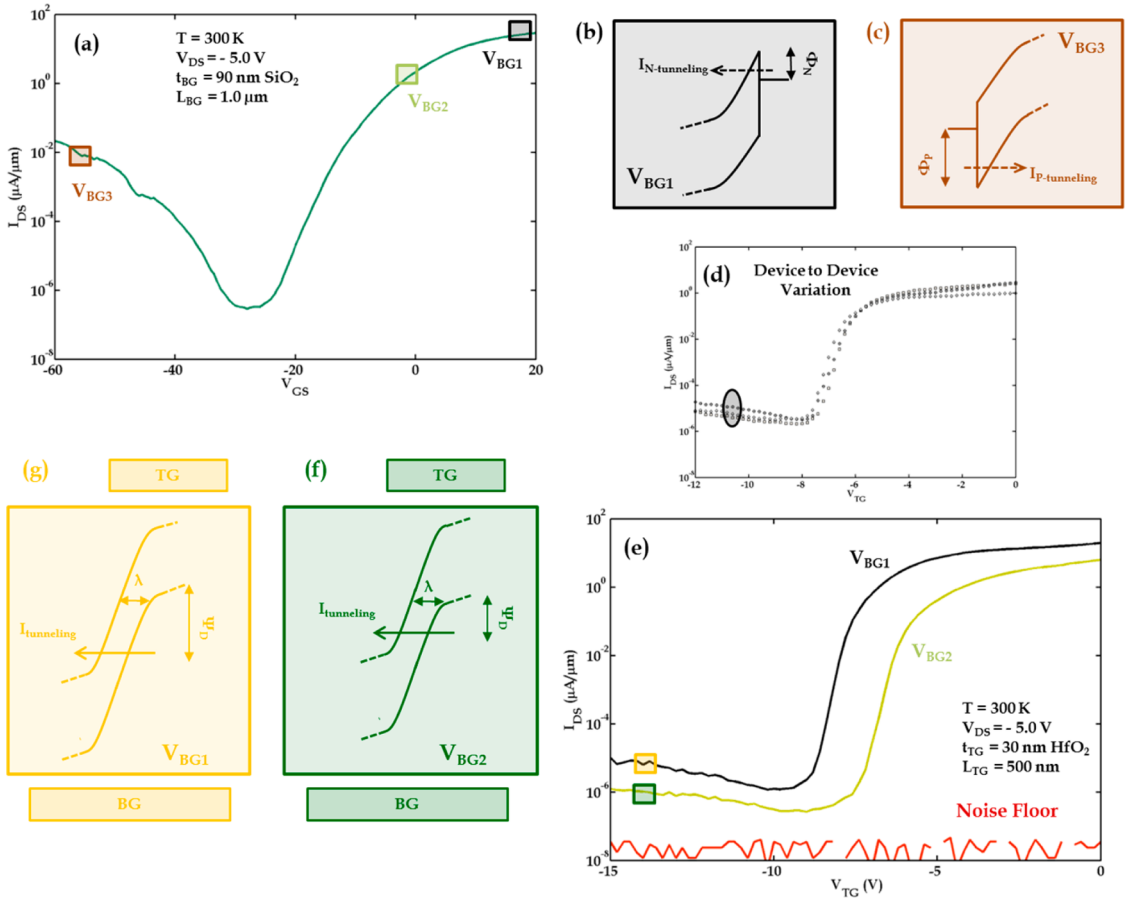


Figure 4. (a) Back gate transfer characteristics of a ~5 nm thick WSe_2 FET. (b,c) Energy band diagrams corresponding to electron injection from the drain terminal and hole injection from the source terminal for the back gate biases V_{BG1} and V_{BG3}, respectively. (d) Device-to-device variations for ~5 nm thick WSe_2 top-gated FETs at V_{BG} = 20 V. (e) Top gate transfer characteristics for two different back gate biases V_{BG1} and V_{BG2}. (f,g) Energy band diagrams corresponding to band-to-band tunneling for different combinations of the top gate and the back gate biases.

current may instead be due to holes injected from the source. To eliminate this possible explanation, top gate scans were performed under different back gate biases, V_{BG}. If the current for negative top gate voltages indeed would be a result of hole injection from the source, the current value for the same top gate overdrive voltage ($V_{TG}-V_{min}$, where V_{min} is the point of minimum current) for V_{BG2} = 0 would be greater than the current value for V_{BG1} = 20 V, which is not the case here. In fact, the observed trend is opposite. This behavior is expected for band-to-band tunneling where a larger current can flow from the valence band by tunneling into the conduction band if the potential difference in the p-n junction region is increased.

In order to further evaluate the observed band-to-band tunneling current, we have used the analytical expressions shown in eq 2.

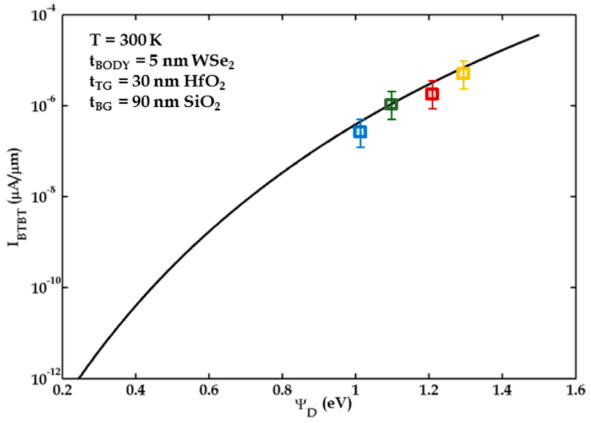
$$I_{\text{tunneling}} = q\int_0^{\Psi_D} M(\Psi_D - E)T_{WKB}(E)[f_c(E) - f_v(E)]dE \quad (2a)$$

$$f_c(E) = \frac{1}{1+\exp\left(\frac{E}{k_BT}\right)}, \quad f_v(E) = \frac{1}{1+\exp\left(\frac{E+\Psi_D}{k_BT}\right)} \quad (2b)$$

$$T_{WKB}(E) = \exp\left(-\frac{8\pi}{3h}\sqrt{2m_rE_G^3}\,\frac{\lambda}{E_G+\Psi_D}\right) \quad (2c)$$

where f_c and f_v are the occupation probabilities in the n and the p region given by the respective source and drain Fermi distributions. The interband tunneling probability is calculated using WKB approximation since it provides reasonably accurate results when compared with other detailed methods like Bardeen's transfer Hamiltonian, Landau−Zener approach *etc.* m_r is the reduced effective mass calculated as the harmonic mean of the electron (m_n) and the hole (m_p) effective masses.[39] The screening length λ is described by a similar expression as in eq 1f but with the difference that $\varepsilon_{\text{environment}}$ needs to be calculated as the average of the dielectric constant of the channel material, the top gate oxide, and the back gate oxide. Finally, $\Psi_D = q|(V_{TG} - V_{FB\text{-}TG})|/\gamma_{TG} + q|(V_{BG} - V_{FB\text{-}BG})|/\gamma_{BG} - E_G$, where γ_{TG} and γ_{BG} are the band movement factors and $V_{FB\text{-}TG}$ and $V_{FB\text{-}BG}$ are the flat band voltages corresponding to the top gate and the back gate biases, respectively.

Figure 5 shows the band-to-band tunneling currents as calculated from eqs 2 as a function of Ψ_D for a



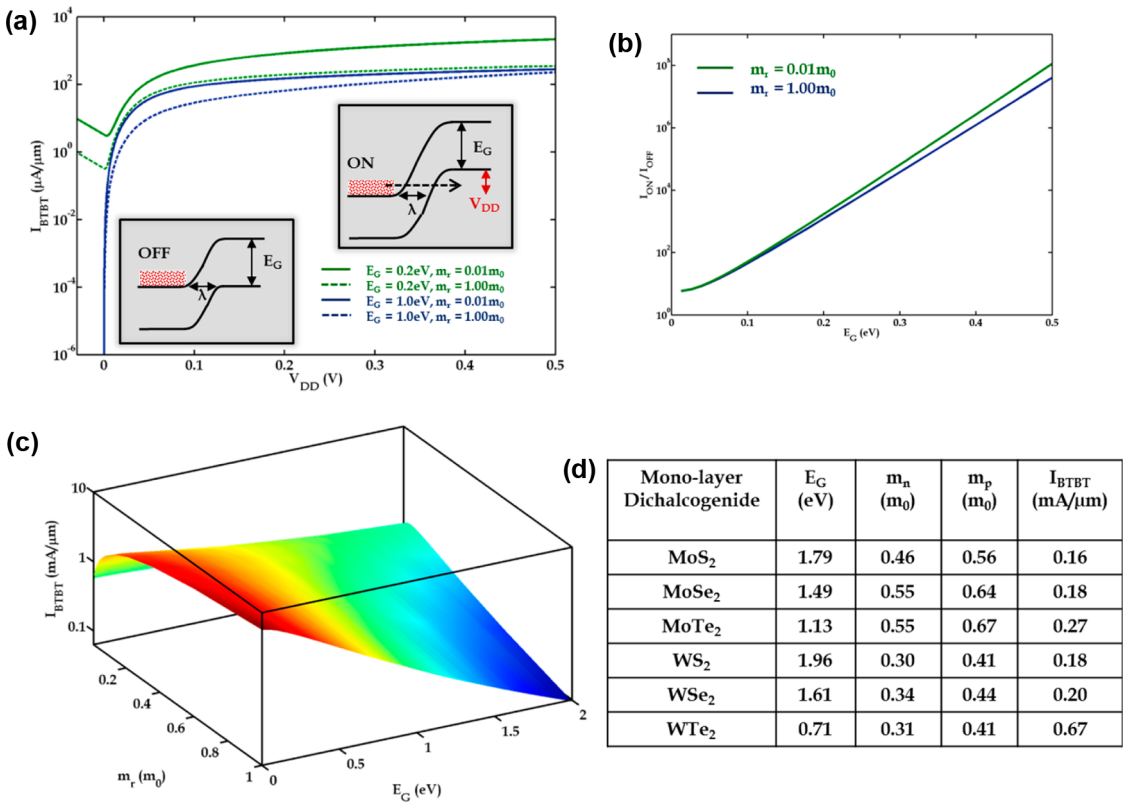
V_{BG} (V)	V_{TG} (V)	Ψ_D (eV)	I_{BTBT} (pA/μm)
20	-13.8	1.25	8.12
10	-13.8	1.19	3.89
0	-13.8	1.09	1.12
-10	-13.8	1.02	0.32

Figure 5. Calculated band-to-band tunneling current levels in WSe_2 p-n junctions are shown as a function of the bias potential Ψ_D. The blue, green, red, and yellow boxes are experimentally extracted data points corresponding to V_{BG} = 20, 10, 0, and −10 V, respectively, as shown in the table.

5 nm thick WSe_2 flake with 30 nm HfO_2 as top gate and 90 nm SiO_2 as the back gate. From our experimental data, we can extract all the parameters required to calculate Ψ_D as described above. For example, we find that for V_{BG} = 20 V and V_{TG} = −13.8 V, Ψ_D = 1.3 eV, and for V_{BG} = 0 V and V_{TG} = −13.8 V, Ψ_D = 1.1 eV. The band-to-band tunneling current corresponding to these two bias points are ∼8 × 10^{-6} and ∼1 × 10^{-6} μA/μm, respectively (yellow and green semitransparent boxes in Figure 4b). The magnitude of the tunneling currents corresponding to different back gate and top gate voltages are also tabulated in Figure 5. Note that the experimental data agree well with the simulated characteristics, as shown in Figure 5.

The reader should note that with large back gate voltages it is possible to create an n-type contact underneath the metallic drain electrode at the SiO_2−TMD interface. It has been widely observed in the case of graphene, which has a low density of states. There is no evidence of such gated contact area for the TMDs. In case such scenario does exist, the tunneling current extracted in this article would be a product of two tunneling probabilities, one at the channel p-n junction and the other at the contact p-n junction. The reader should also note that both the back gate and the top gate, in our partially gated WSe_2 FET, have complete control of the WSe_2 stack. This is evident from the transfer characteristics (Figure 4a,e) that clearly show that both the back and the top gate can individually turn the device off. Therefore, all the layers in our multilayer WSe_2 stack are under tight gate control (both top and back). Under different combinations of the top and the back gate bias, the entire stack is either n- or p-type-doped. A variable doping profile among the layers cannot exist which eliminates the possibility of interlayer tunneling transverse to the channel direction.

Projections for Band-to-Band Tunneling Currents in TMDs. Since our experimental data can be explained within reasonable degree of accuracy by our simple analytical models, we use the same to make projections for band-to-band tunneling (BTBT) currents in transition metal dichalcogenide p-n homojunctions (see inset of Figure 6a) which are the basic building blocks for TFETs. One of the major obstacles in the implementation of TFET is its poor drive current capability limited by the transmission through large tunneling barriers that exist in these p-n junctions. The tunneling current in such p-n junction is given by the set of eqs 2 with Ψ_D being replaced by the applied bias qV_{DD} if we assume that scattering inside the p or n channel does not impact the current. As evident from the equations, thinner gate oxides and thinner channels are desired to reduce the magnitude of λ and hence increase the tunneling probability. Layered two-dimensional dichalcogenides with ultrathin body thicknesses are, therefore, desirable in the context of TFETs as significantly higher tunneling current densities could be achieved. Material parameters like the band gap (E_G) and the effective mass (m_r) also play an equally important role in determining the tunneling probability. Figure 6a shows the band-to-band tunneling currents (I_{BTBT}) as a function of the bias voltage V_{DD} in logarithmic scale based on hypothetical 2-D materials (d_{body} = 1 nm) with different combinations of band gap (E_G) and reduced effective mass (m_r). The effective oxide thickness (EOT) was assumed to be 1 nm. As seen in Figure 6a, smaller band gaps improve the on-state drive current density but at the expense of a degraded off-state performance. This is because in this case a substantial thermionic emission current can flow from the n region to the p region. Figure 6b shows that the ratio of the on-state band-to-band tunneling current to the off-state thermionic emission current changes exponentially as a function of E_G for any given m_r. Figure 6b also suggests that the on−off ratio is not impacted significantly by the effective mass. Figure 6c shows the on-state drive current density as a function of both m_r and E_G. It is interesting to note that there exists a local maximum for the drive current density as a function of the effective mass corresponding to each different band gap. This local maximum is an outcome of two



Mono-layer Dichalcogenide	E_G (eV)	m_n (m_0)	m_p (m_0)	I_{BTBT} (mA/μm)
MoS_2	1.79	0.46	0.56	0.16
$MoSe_2$	1.49	0.55	0.64	0.18
$MoTe_2$	1.13	0.55	0.67	0.27
WS_2	1.96	0.30	0.41	0.18
WSe_2	1.61	0.34	0.44	0.20
WTe_2	0.71	0.31	0.41	0.67

Figure 6. (a) Band-to-band tunneling current (I_{BTBT}) in logarithmic scale as a function of the bias V_{DD} for different combinations of band gaps and effective masses. The cartoons in the inset show the basic operation principal. (b) Ratio of on-state tunneling current to the off-state thermionic current as a function of the band gap for different effective masses. (c) Band-to-band tunneling current for a given bias V_{DD} = 0.5 V as a function of both the effective mass and the band gap. (d) Table shows the band gap, electron, and hole effective masses and I_{BTBT} for 0.5 V supply voltage for various monolayer TMDs calculated using the model described in the text.

counteracting effects—smaller values for m_r improve the tunneling probability but at the same time reduce the number of conducting modes. Since the tunneling current is a product of the number of conducting modes and the tunneling probability, a local maximum exists for each E_G. Given the requirement for CMOS logic circuit design which demands a minimum on−off ratio of 10^4, the band gap E_G should be chosen to be larger than 0.3 eV.

The above-described situation is, however, far from reality where E_G and m_r are coupled through the energy dispersion relationship and, therefore, cannot be tuned independently for any material. Also for the same material, these parameters depend strongly on the body thickness. The table in Figure 6d shows the magnitude of the band gap (E_G), electron effective mass (m_n), and hole effective mass (m_p)[40,41] and the corresponding band-to-band tunneling currents for V_{DD} = 0.5 V in a p-n homojunction made from various monolayer transition metal dichalcogenides. Note that the effective mass m_r has been calculated as the harmonic mean of m_n and m_p. Monolayer WTe_2, by the virtue of its smaller band gap, outperforms all other dichalcogenides with I_{BTBT} of ~0.67 mA/μm. Among the dichalcogenides which have been widely studied as the channel material for field-effect transistors, WSe_2 and $MoTe_2$ appear to be better choices for tunneling applications. Our analysis provides initial basic insights into the material parameters that are important in the context of tunneling and thereby helps in identifying the ideal 2-D material for TFET applications.

CONCLUSION

In conclusion, we experimentally demonstrated for the first time hole tunneling currents through triangular Schottky barriers in MoS_2 back-gated FETs and band-to-band tunneling currents in double-gated WSe_2 FETs. We found that by scaling the geometric screening length λ, the tunneling current can be increased by orders of magnitude. Finally, we also used our experimental data and analytical calculations to provide projections for band-to-band tunneling currents for monolayer dichalcogenides.

METHODS

MoS_2 flakes were mechanically exfoliated onto 20 and 100 nm silicon dioxide substrates with underlying highly doped silicon. Flake thicknesses were first identified approximately through optical contrast and then accurately determined by atomic force microscopy. Electron beam lithography followed

by electron beam evaporation was used to define source/drain contact electrodes. A 50 nm thick layer of palladium with a subnanometer adhesive layer of titanium was used as the source/drain metal contact.

A fabrication process similar to the one described above for MoS_2 FETs was used to create back-gated WSe_2 FETs with Ti/Pd contacts on a 90 nm SiO_2 substrate with underlying highly doped silicon. Flakes thicknesses ~5 nm thick were selected for the fabrication of the band-to-band tunneling devices. The 30 nm HfO_2 was deposited as the top gate dielectric using atomic layer deposition techniques.

Conflict of Interest: The authors declare no competing financial interest.

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